an SOI substrate having a structure in which a semiconductor substrate, an insulating layer and a semiconductor layer are layered in this order, the semiconductor substrate being in contact with the insulating layer;

a partial-isolation insulating film formed in a main surface of said semiconductor layer;

a first semiconductor element formed in an element formation region defined by said partial-isolation insulating film in said semiconductor layer, said first semiconductor element including source/drain regions formed in contact with said insulating layer;

an interlayer insulating film formed on said first semiconductor element and said partial-isolation insulating film;

at least one of a power supply line and a ground line formed on said interlayer insulating film; and

a first complete-isolation insulating film formed throughout a portion directly below at least one of said power supply line and ground line.

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## REMARKS

Favorable reconsideration of this application is respectfully requested.

Claims 1-20 are pending in this application. Claims 2-20 stand withdrawn from consideration. Claim 1 was rejected under 35 U.S.C. § 103(a) as unpatentable over U.S. patent 6,118,152 to Yamaguchi et al. (herein "Yamaguchi") in view of U.S. patent 5,747,846 to Iida et al. (herein "Iida").

Initially, applicant and applicants' representative wish to thank Examiner Tran for the interview granted on April 7, 2003. During that interview the outstanding rejections were discussed in detail. Further, during that interview claim amendments were discussed to clarify the claims over the applied art. The present response sets forth different claim

amendments than as discussed, but the amended claims are believed to also distinguish over the applied art.

Addressing the rejection to claim 1 over Yamaguchi in view of Iida, that rejection is traversed by the present response.

It is initially noted that claim 1 is amended by the present response to clarify features recited therein. First, independent claim 1 clarifies "the semiconductor substrate being in contact with the insulating layer". Claim 1 now also recites "said first semiconductor element including source/drain regions formed in contact with said insulating layer". That subject matter is supported for example in Figures 2 and 22 in the specification. In Figure 2 in the specification the top surface of a semiconductor substrate 2 is shown formed in contact with the bottom surface of insulating layer 3. Also, in Figure 22 the bottom surfaces of source/drain regions 28 are shown in contact with the top surface of an insulating layer 3. The features now clarified in the above-noted claims are believed to distinguish over the applied art.

In Figure 1 of Yamaguchi an impurity-doped polysilicon layer 2 is formed between a semiconductor substrate 1 and an insulating layer 3. As a result noise enters from a ground wiring 19a and travels through the polysilicon layer 2 and the insulating layer 3 to a body region of a transistor.

In contrast to Yamaguchi, in claim 1 a semiconductor substrate is formed in contact with an insulating layer, and therefore it is possible to prevent the above-noted type of noise.

Further, as shown in Figures 2-7 of Yamaguchi the method of manufacturing the device of Yamaguchi is very complicated and requires many factoring steps. The semiconductor device according to claim 1 allows manufacturing steps to be reduced as compared with the device of Yamaguchi, thereby improving yields.

Further, no teachings in Iida can overcome the deficiencies in Yamaguchi. In Figure 1 of Iida when a noise enters a silicon region that is directly below a gate electrode 51, the noise travels through a p type gate region 5 to a transistor Ts, and the transistor Ts is adversely effected.

In contrast to Iida, in claim 1 the source/drain regions are in contact with the insulating layer, and therefore it is possible to prevent noise that travels from a lateral direction as noted above.

Further, in the device of Figure 1 of Iida because the source/drain regions 34-38 are not in contact with insulating layer 2, junction capacity is increased and the working speed of the transistor is reduced. Moreover, because the device includes an $N^-$ layer 3 and an $N^+$ layer 4, many manufacturing steps are required.

In contrast to Iida in claim 1 the source/drain regions are in contact with the insulating layer, and therefore it is possible to reduce junction capacity, thereby allowing working speed of the transistor to be increased as compared with the device of Iida. Moreover, because there is no need for forming the $N^-$layer 3 and the $N^+$ layer 4 as in Iida, it is possible to reduce manufacturing steps as compared with the device of Iida.

In such ways, independent claim 1 is believed to distinguish over the applied art.

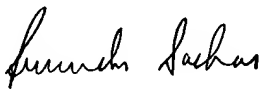
It is also noted that each of claims 2-7 depends from independent claim 1, and thus independent claim 1 is clearly generic to each of claims 2-7. Therefore, each of claims 2-7 must now be rejoined.

Thus, each of claims 1-7 is now in condition for allowance.

As no other issues are pending in this application, it is respectfully submitted that the present application is now in condition for allowance, and it is hereby respectfully requested that this case be passed to issue.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.



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IN THE TITLE

SEMICONDUCTOR DEVICE [AND METHOD OF MANUFACTURING THE SAME]

IN THE CLAIMS

--1. (Three Times Amended) A semiconductor device comprising:

an SOI substrate having a structure in which a semiconductor substrate, an insulating layer and a semiconductor layer are layered in this order, the semiconductor substrate being in contact with the insulating layer;

a partial-isolation insulating film formed in a main surface of said semiconductor layer;

a first semiconductor element formed in an element formation region defined by said partial-isolation insulating film in said semiconductor layer, said first semiconductor element including source/drain regions formed in contact with said insulating layer;

an interlayer [insulting] insulating film formed on said first semiconductor element and said partial-isolation insulating film;

at least one of a power supply line and a ground line formed on said interlayer insulating film; and

a first complete-isolation insulating film formed throughout a portion directly below at least one of said power supply line and ground line.--